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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TRAN, THANH Y	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 04/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/828,495	PARTRIDGE ET AL.	
	Examiner	Art Unit	
	Thanh Y. Tran	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 9-11, and 21-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Komiyama (U.S 6,329,708).

As to claim 9, Komiyama discloses in figure 8 a high-density circuit module comprising: a first CSP ("semiconductor chip" 701b); a second CSP ("semiconductor chip" 701a) stacked above the first CSP ("semiconductor chip" 701b); a first form standard ("insulating layer" 709b) associated with the first CSP ("semiconductor chip" 701b); and a second form standard ("insulating layer" 709a) associated with the second CSP ("semiconductor chip" 701a); and flex circuitry ("conductive layer" 710b) comprising a first side and a second side and a covercoat ("insulating layer" 713b) on each of the first and second sides.

As to claim 10, Komiyama discloses in figure 8 a high-density circuit module comprising: flex circuitry ("conductive layer" 710b) connecting the first and second CSPs (semiconductor chips 701b, 701a).

As to claim 11, Komiyama discloses in figure 8 a high-density circuit module wherein the flex circuitry ("conductive layer" 710b) is comprised of first and second flex circuits [*a first flex circuit is a flex circuit ("conductive layer" 710b) on right side of semiconductor chip 701b,*

and a second flex circuit is a corresponding flex circuit ("conductive layer" 710b) on the opposite side or the left side of semiconductor chip 701b].

As to claim 21, Komiyama discloses in figure 8 a stacked circuit module comprising: a CSP ("semiconductor chip" 701b); a form standard ("insulating layer" 709b) attached to the CSP ("semiconductor chip" 701b); and flex circuitry ("conductive layer" 710b) attached to the form standard ("insulating layer" 709b), and comprising a first side and a second side and a covercoat ("insulating layer" 713b) on each of the first and second sides.

As to claim 22, Komiyama discloses in figure 8 a stacked circuit module wherein the flex circuitry ("conductive layer" 710b) is comprised of first and second flex circuits [*a first flex circuit is a flex circuit ("conductive layer" 710b) on right side of semiconductor chip 701b, and a second flex circuit is a corresponding flex circuit ("conductive layer" 710b) on the opposite side or the left side of semiconductor chip 701b*].

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-4, 12, 16-18, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Komiyama et al (U.S. 6,329,708) in view of Pan (U.S. 6,588,095).

As to claim 1, Komiyama discloses in figure 8 a high-density circuit module comprising: a first CSP ("semiconductor chip" 701b); a second CSP ("semiconductor chip" 701a) disposed

above the first CSP ("semiconductor chip" 701b) in stacked disposition; a first form standard ("insulating layer" 709b) disposed, in substantial part, above the first CSP ("semiconductor chip" 701b); flex circuitry ("conductive layer" 710b) connecting the first and second CSPs (semiconductor chips 701b, 701a) and positioned to be, in part, beneath the first CSP ("semiconductor chip" 701b) and, in part, above the first form standard ("insulating layer" 709b) and beneath the second CSP ("semiconductor chip" 701a), the flex circuitry ("conductive layer" 710b) comprising a first side and a second side and a covercoat ("insulating layer" 713b) on each of the first and second sides.

Komiyama does not disclose the flex circuitry is attached to the first form standard with at least one metallic bond.

Pan discloses in figure 2 a high-density circuit module wherein a flex circuitry ("flex circuit" 15) is attached to the first form standard ("thin film" 19) with at least one metallic bond ("conductive bonding beam" 16) (see col. 3, lines 20-62). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the circuit module of Komiyama by using at least one metallic bond material as taught by Pan for providing a thermally conductive connection between the flex circuitry and the chips/CSPs.

As to claim 2, Komiyama discloses in figure 8 a high-density circuit module further comprising: a second form standard disposed ("insulating layer" 709a), in substantial part, above the second CSP ("semiconductor chip" 701a).

As to claims 3, 12 and 23, Komiyama discloses in figure 8 a high-density circuit module wherein the flex circuitry is comprised of a first flex circuit [*a first flex circuit is a flex circuit ("conductive layer" 710b) on the right side of the semiconductor chip 701b, and a second flex*

circuit [a second flex circuit is a corresponding flex circuit ("conductive layer" 710b) on the opposite side or the left side of semiconductor chip 701b].

Komiyama does not disclose each of the flex circuitry is attached to the first form standard with at least one metallic bond.

Pan discloses in figure 2 a high-density circuit module wherein a flex circuitry ("flex circuit" 15) is attached to the first form standard ("thin film" 19) with at least one metallic bond ("conductive bonding beam" 16) (see col. 3, lines 20-62). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the circuit module of Komiyama by using at least one metallic bond material as taught by Pan for providing a thermally conductive connection between the flex circuitry and the chips/CSPs.

As to claims 4 and 16, Komiyama discloses in figure 8 a high-density circuit module further comprising: a second form standard ("insulating layer" 709a) and in which the flex circuitry ("conductive layer" 710b) is comprised of a first flex circuit [*a first flex circuit is a flex circuit ("conductive layer" 710b) on right side of semiconductor chip 701b*], and a second flex circuit [*a second flex circuit is a corresponding flex circuit ("conductive layer" 710b) on the opposite side or the left side of semiconductor chip 701b*].

Komiyama does not disclose each of flex circuit is attached to the first form standard with at least one metallic bond.

Pan discloses in figure 2 a high-density circuit module wherein a flex circuitry ("flex circuit" 15) is attached to the first form standard ("thin film" 19) with at least one metallic bond ("conductive bonding beam" 16) (see col. 3, lines 20-62). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the

circuit module of Komiyama by using at least one metallic bond material as taught by Pan for providing a thermally conductive connection between the flex circuitry and the chips/CSPs.

As to claim 17, Komiyama does not disclose each of the flex circuit is attached to the first form standard with adhesive. Pan discloses in figure 2 a high-density circuit module wherein a flex circuitry ("flex circuit" 15) is attached to the first form standard ("thin film" 19) with adhesive ("conductive bonding beam" 16). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the circuit module of Komiyama by using adhesive material as taught by Pan for providing a thermally conductive connection between the flex circuitry and the chips/CSPs.

As to claim18, Komiyama discloses in figure 8 a high-density circuit module and a corresponding method comprising: providing a form standard ("insulating layer" 709b); providing first and second CSPs (semiconductor chips 701b, 701a); attaching the form standard ("insulating layer" 709b) to the first CSP ("semiconductor chip" 701b); providing flex circuitry ("conductive layer" 710b) comprising a first side and a second side and a covercoat ("insulating layer" 713b) on each of the first and second sides with an area; disposing the flex circuitry ("conductive layer" 710b) adjacent to the first form standard ("insulating layer" 709b) to create an area of contact (i.e. an area of contact with a metal bump 703).

Komiyama does not disclose the step of: applying a first metallic material to at least one part of the first form standard; and selectively applying heat to the area of contact.

Pan discloses in figure 2 a high-density circuit module wherein a flex circuitry ("flex circuit" 15) is attached to the first form standard ("thin film" 19) with a first metallic material ("conductive bonding beam" 16); and the first metallic material ("conductive bonding beam" 16)

is inherent for selectively applying heat to the area of contact (pad 14) [bonding beam 16 is inherent for selectively applying heat to the area of contact (pad 14) because bonding beam 16 is a conductive material]. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the circuit module of Komiyama by applying a first metallic material to at least one part of the first form standard; and selectively applying heat to the area of contact as taught by Pan for providing a thermally conductive connection between the flex circuitry and the chips/CSPs.

5. Claims 5-8, 13-15, 20 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Komiyama et al (U.S. 6,329,708) in view of Pan (U.S. 6,588,095) as applied to claim 1 above, and further in view of Komota (U.S. 2003/0016710).

As to claims 5, 20 and 24, Komiyama in view of Pan does not disclose the metallic bond comprises at least two metals or tin and gold; the first metallic material is comprised of tin. Komota discloses a metallic bond (adhesive) comprises at least two metals (tin and gold); the first metallic material is comprised of tin (see paragraph [0058]). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the module of Komiyama in view of Pan by using a metallic bond (adhesive) comprises at least two metals (tin and gold) as taught by Komota for providing a reliable bond formation because known tin and gold materials have high thermal melting bond.

As to claim 6, Komiyama in view of Pan does not disclose a metallic bond is created by combining a first metallic material applied to the first form standard and a second metallic material from which the flex circuitry is comprised. Komota discloses a metallic bond

(adhesive) comprises tin and gold materials (see paragraph [0058]). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the module of Komiyama in view of Pan by using a metallic bond (adhesive) comprises tin (first metallic material) and gold (second metallic material) as taught by Komota for providing a reliable bond formation because known tin and gold materials have high thermal melting bond.

Further, the limitation of "metallic bond is created *by combining a first metallic material applied to the first form standard and a second metallic material from which the flex circuitry is comprised*" is a process limitation in a product claim which does not otherwise patentably distinguish over prior art, cannot impart patentability to the product. In re Stephens 145 USPQ 656 (CCPA "thin film" 1965).

As to claims 7, 8, and 15, Komiyama in view of Pan does not disclose the combining of the first metallic material and the second metallic material is achieved through a selected application of heat. Komota discloses a metallic bond (adhesive) comprises tin (first material) and gold (second material) is achieved through a selected application of heat and is achieved with localized friction heating (see paragraph [0058]) (it should be noted that: when a metallic bond (adhesive) is heated it is inherently achieved through a selected application of heat and is achieved with localized friction heating). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the module of Komiyama in view of Pan by using a metallic bond (adhesive) comprises tin (first metallic material) and gold (second metallic material) as taught by Komota for providing a reliable bond formation because known tin and gold materials have high thermal melting bond.

Further, the limitations of "the combining of the first metallic material and the second metallic material is achieved through a selected application of heat" in claim 7, and "the selected application of heat is achieved with localized friction heating" in claim 8, "the metallic bond *is realized by selective application of heat*" in claim 15 are process limitations in product claims which do not otherwise patentably distinguish over prior art, cannot impart patentability to the product. In re Stephens 145 USPQ 656 (CCPA "thin film" 1965).

As to claims 13 and 14, Komiyama in view of Pan does not disclose the metallic bond comprises a first metallic material and a second metallic material. Komota discloses a metallic bond (adhesive) comprises a first metallic material (tin) and a second metallic material (gold) (see paragraph [0058]). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the module of Komiyama in view of Pan by using a metallic bond (adhesive) comprises a first metallic material (tin) and a second metallic material (gold) as taught by Komota for providing a reliable bond formation because known tin and gold materials have high thermal melting bond.

6. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Komiyama et al (U.S. 6,329,708) in view of Pan (U.S. 6,588,095) as applied to claim 1 above, and further in view of Chiang (U.S. 6,803,651).

As to claim 19, Komiyama et al in view of Pan does not teach step of using vibration to perform the step of selectively applying heat to the area of contact. Chiang teaches the method of using vibration to perform the step of selectively applying heat to the area of contact (see col. 13, lines 7-10). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus and the corresponding method of

Komiyama in view of Pan by using vibration method for performing heat as taught by Chiang for providing a good bonding connection which is easy to be deformed by vibration (see col. 13, lines 7-10 in Chiang).

7. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Komiyama et al (U.S. 6,329,708) in view of Nicewarner, Jr. et al (U.S. 5,776,797) and Pan (U.S. 6,588,095).

As to claim 26, Komiyama discloses in figure 8 a high-density circuit module comprising: a first CSP ("semiconductor chip" 701b); a second CSP ("semiconductor chip" 701a) disposed above the first CSP ("semiconductor chip" 701b) in stacked disposition; a first form standard ("insulating layer" 709b) disposed, in substantial part, above the first CSP ("semiconductor chip" 701b); flex circuitry ("conductive layer" 710b) connecting the first and second CSPs (semiconductor chips 701b, 701a) and positioned to be, in part, beneath the first CSP ("semiconductor chip" 701b) and, in part, above the first form standard ("insulating layer" 709b) and beneath the second CSP ("semiconductor chip" 701a),

Komiyama does not disclose the flex circuitry comprising at least two conductive layers.

Nicewarner discloses in figure 3 an apparatus wherein the flex circuitry comprising at least two conductive layers (40, 42). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Komiyama by having a flex circuitry which comprises at least two conductive layers as taught by Nicewarner for the purpose of providing an electrical interconnection between the at least two chips (see col. 1, lines 55-65 in Nicewarner).

Komiyama in view of Nicewarner does not disclose the flex circuitry is attached to the

first form standard with at least one metallic bond.

Pan discloses in figure 2 a high-density circuit module wherein a flex circuitry ("flex circuit" 15) is attached to the first form standard ("thin film" 19) with at least one metallic bond ("conductive bonding beam" 16) (see col. 3, lines 20-62). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the circuit module of Komiyama in view of Nicewarner by using at least one metallic bond material as taught by Pan for providing a thermally conductive connection between the flex circuitry and the chips/CSPs.

8. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Komiyama et al (U.S. 6,329,708) in view of Nicewarner, Jr. et al (U.S. 5,776,797).

As to claim 27, Komiyama discloses in figure 8 a unit for use in a stacked circuit module comprising: a CSP ("semiconductor chip" 701b); a form standard ("insulating layer" 709b) attached to the CSP (701b); and flex circuitry ("conductive layer" 710b) attached to the form standard ("insulating layer" 709b).

Komiyama does not disclose the flex circuitry comprising at least two conductive layers.

Nicewarner discloses in figure 3 an apparatus wherein the flex circuitry comprising at least two conductive layers (40, 42). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Komiyama by having a flex circuitry which comprises at least two conductive layers as taught by Nicewarner for the purpose of providing an electrical interconnection between the at least two chips (see col. 1, lines 55-65 in Nicewarner).

Response to Arguments

9. Applicant's arguments with respect to claims 1, 3-4, 9-12, 16, 18, 21-23, and 26-27 have been considered but are moot in view of the new ground(s) of rejection.

Applicant argued that "insulating layers" 709a and 709b of Komiyama, and "thin film" 19 of Pan are not "form standards".

In response, the examiner disagrees with applicant's argument because "a form standard" is known in the art, and it can be a base or holder or supporter for holding or supporting an element (e.g., a flex circuitry). Komiyama clearly discloses in figure 8 "insulating layers" 709a and 709b supporting the flex circuitry ("conductive layer" 710a and 710b); and Pan clearly discloses in figure 2 "thin film" 19 supporting the flex circuitry (15). Applicant has never recited "a form standard" has any specific structure that at least discloses the difference from the structures of the form standards of Komiyama and Pan. Thus, "insulating layers" 709a and 709b of Komiyama, and "thin film" 19 of Pan are treated as "form standards" for supporting the flex circuits.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Y. Tran whose telephone number is (571) 272-2110. The examiner can normally be reached on M-F (9-6:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith, can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9"thin film" 197 (toll-free).

TYT

Zandra V. Smith
Supervisory Patent Examiner
3 April 2006